Listing of Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1-11. (Previously cancelled)

12. (previously added) A method for fabricating a low resistance interconnect line in an integrated circuit, the method comprising the steps of:

forming a dielectric layer on a substrate of an integrated circuit,

patterning and etching the dielectric layer to form a trench, wherein the patterning is performed using a first photomask;

filling the trench in the dielectric layer with copper;

polishing the copper and the dielectric to form a first planarized surface comprising a top polished surface of the copper and a top polished surface of the dielectric, wherein the top polished surface of the copper and the trench define a lower conductive metal portion of the interconnect line, the lower conductive metal portion comprising copper;

depositing an aluminum layer on at least a portion of the top polished surface of the dielectric and at least a portion of the top polished surface of the copper of the first planarized surface; and

patterning and etching the aluminum to define an upper conductive metal portion of the interconnect line, wherein the upper conductive metal portion is further defined so that the aluminum overlies the lower conductive metal portion.

13. (currently amended) The method for fabricating low resistance interconnect lines as recited in claim 12 wherein the first photomask is used to pattern the aluminum layer to define the upper conductive metal portion of the interconnect using a photoresist layer having ~~in~~ a tone reversed from that used for patterning and etching the dielectric.

14. (previously added) The method for fabricating low resistance interconnect lines as recited in claim 12 wherein the low resistance interconnect comprises two layers of conductive metal over its length between a first connection point and a second connection point in the integrated circuit, wherein the lower conductive metal layer comprises copper and the upper conductive metal layer comprises aluminum.

15. (previously added) The method for fabricating low resistance interconnect lines as recited in claim 12 wherein the aluminum layer is deposited directly on the first planarized surface.

16. (previously added) The method for fabricating low resistance interconnect lines as recited in claim 12 further comprising depositing a barrier layer directly on the first planarized surface.

17. (previously added) The method for fabricating low resistance interconnect lines as recited in claim 16 wherein the aluminum layer is deposited directly on the barrier layer.

18. (previously added) The method for fabricating low resistance interconnect lines as recited in claim 16 wherein the barrier layer is at least one of Ta or TaN ranging from 0.005 to 0.050 μm in thickness.

19. (previously added) The method for fabricating low resistance interconnect lines as recited in claim 18 wherein the copper has a thickness within the range of 0.3 to 2.0 μm and the aluminum has a thickness within the range of 0.5 to 3.0 μm.

20. (previously added) The method for fabricating low resistance interconnect lines as recited in claim 12 wherein the copper has a thickness within the range of 0.3 to 2.0 μm and the aluminum has a thickness within the range of 0.5 to 3.0 μm.

21. (previously added) The method for fabricating low resistance interconnect lines as recited in claim 20 wherein the thickness of the copper and the thickness of the aluminum are adjusted so that the completed interconnect line has a first predefined electrical resistance within the range of 0.012 to 0.008 Ω per unit length.

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22. (new) The method for fabricating low resistance interconnect lines as recited in claim 14 wherein each of the first and second connection points comprises an electrical connection with one of a via, a bonding pad, and a contact.

23. (new) A method for fabricating a low resistance dual metal interconnect line in an integrated circuit, the method comprising:

exposing the planarized surface of a copper interconnect line formed by a damascene method in a dielectric layer of a semiconductor wafer;

depositing an aluminum pad metal layer on the planarized surface;

patterning and etching the aluminum pad metal layer to define an upper conductive metal portion of a dual metal interconnect line, the copper interconnect forming the lower metal portion of the dual metal interconnect line.

24. (new) The method of forming a low resistance interconnect line as recited in claim 23 wherein the same photomask used to pattern the dielectric layer to form the copper interconnect line is used to pattern the aluminum pad metal layer.

25. (new) The method of forming a low resistance interconnect line as recited in claim 23 wherein a photomask is used to pattern the dielectric layer to form the copper interconnect line and is used to pattern the aluminum pad metal layer to define the upper conductive metal portion of the interconnect by using a photoresist layer having a tone reversed from that used for patterning the dielectric layer.

26. (new) The method of forming a low resistance interconnect line as recited in claim 23 further comprising patterning and etching the pad metal layer to define a conductive pad configured to provide one of input and output connections to the integrated circuit.

27. (new) The method of forming a low resistance interconnect line as recited in claim 23 wherein the copper has a thickness within the range of 0.3 to 2.0 μm and the aluminum has a thickness within the range of 0.5 to 3.0 μm. and the thickness of the copper and the thickness of the aluminum are adjusted so that the completed interconnect line has a first predefined electrical resistance within the range of 0.012 to 0.008 Ω per unit length.